Packaging Solutions using MIS Platform
Outline

◆ MIS Technology Introduction

◆ Advanced MIS Package solutions
  • MIS Ultra-thin package
  • MIS Multilayer package
  • 3D MIS package
  • MIS SIP module package

◆ Summary
Internet of Things – Broad Prospective

- 5 Key Verticals of Adoption

1. Connected Homes
2. Mobile & Wearables
3. Connected Vehicles
4. Smart Power Grid
5. Transportation & Container Track

- Connected Cities
- Home Appliance Infotainment Security
- Traffic/Parking/Toll
- Activities Center
- Oil & Gas & Power
- Healthcare
- Environment

- Agriculture
- Transit

JCET Confidential
Technology Innovations

Processor
Memory
Sensors
WiFi / Wireless
Interface Display
Power Source
Semiconductor IC for IoT

- Minaturisation and Advanced in Packaging Technologies -wearable
- Advances in Flash
- New Class of powerful, but low cost and ultra-low power MCUs
- Faster and ultra-low power Wireless Communication
Complexity of semiconductor IC designs
- Increase functionalities of consumer electronics, there is an increasing need for multifunctional ICs.
  sophisticated architecture and designs for semiconductor ICs
- At the same time – needs to be low Power, high signal integrity

Increasing miniaturization of electronic devices
- The increasing demand for compact electronic devices used in multiple sectors like Mobile & Wearables and automotive has led to further miniaturization of semiconductor ICs.
- With advances in technology like 3D ICs and MEMS, as well as changes in the design of ICs such as finer patterning, electronic equipment is becoming more compact and user-friendly.
- MEMS is a technology used for miniaturization of chips by the process of microfabrication.
Semiconductor IC Packaging using MIS

- High Rel. MSL 1
- Heat sink Cu Pillar
- Ultra Thin Min. 90um
- MIS Platform
  - Trace
  - External lead
  - Pre-mold compound
- High performance Embedded
- Fine pitch 12/12um
• MIS Package
- Structure: FC-BGA

✓ Technology comparison

<table>
<thead>
<tr>
<th>Higher Cost</th>
<th>Coreless</th>
<th>MSAP</th>
<th>SAP</th>
<th>MIS</th>
<th>ETS</th>
<th>Fan-out/eWLB</th>
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<td>35/35</td>
<td>30/30</td>
<td>25/25</td>
<td>20/20</td>
<td>15/15</td>
<td>10/10um</td>
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Features of MIS

Fine Pitch

- Ultra fine line: L/S 12um — High density package
- MIS vs non-MIS

High Reliability

- Rough Cu surface
  - High reliability MSL-1
  - Low skin effect loss

Embedded Trace

- Embedded line and trace — High reliability

FC-BGA 2L MISBGA

Cu Thermal Stud

- 100% Cu-filled via
- larger via Dia. at same pad
- Good conductivity and thermal performance

Thin Coreless

- Cu and Epoxy composition
- Thin thickness: ≤120um
- High reliability
Features of MIS

FC Die Pad Cu recession Depth(Spec: $5 \pm 3\mu m$)

Cu recession Depth: $4.4\mu m$

Embedded Copper Trace
Top View

FC Die Attach  Pb-free Reflow

NO non-wetting for 13X13mm High Pin-Count Reflow
MIS Platform Package Application

- SOCs, ASICs, Basebands, APs, Logics, Analog, Mixed Signals, RF, PMC, etc.
- Power Management ICs
- RFICs
- Basebands SOC
- Mixed-Signals
- DRAM FC Packages
### MIS Package Roadmap

#### Qualified/Production

<table>
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<tr>
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<th>4Q15</th>
<th>1Q16</th>
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#### Power management/Radio Frequency
- **High Power Package.**
  - MIS trace thickness: Min. 40um
  - MIS total thickness: 127/110um.
- **Ultra thin package**
  - Package thickness: Max. 0.33/0.3mm
  - MIS total thickness: 100/80um.
- **Dual Row QFN Package**

#### Automotive products
- QFN-MIS Sidewall Wettable
  - Thickness: 110um,
  - Depth: 50+-/-10um
- Multi-layer package

#### 3D and SIP Package

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<td><strong>3D and SIP Package</strong></td>
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<td><strong>MIS Substrate</strong></td>
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</table>
- Total thickness : 0.95/1.2mm
- Stack Inductor
- Flip chip die: Cu pillar Bump

#### Computing and Consumer
- 3D MIS Package with RDL
  - 2/3 Layer
  - Flip chip die
  - RDL on 2nd MD(Film)
  - Stack Inductor
- **MIS-SIP PM module**
  - MOSFET/IC
  - Film mold
  - Heat sink

**Blue font = updates to existing project**

**New addition**

**Internal Roadmap only**

**Subject to feasibility/trend verification and final MRS**
• **MIS Ultra-Thin Package**

- Multiple chips, Die Stacked, High Pin Count
- Ultra Thin(X3,X4)
- CAu/PdCu/AuPdCu/Cu/Ag Alloy Wire
- RF, Ultra-loop, Flip chip, SMT integration
• **MIS Ultra-Thin Package**

✓ MIS thinner package milestone

✓ **MIS thinner package solution**

Current 1L MIS(Strip Level with 10um Cu layer)-X2
- Substrate buildup Dielectric film for Cu RDL layers
- Pattern 20/20um
- High breakage, require copper metal layer as additional carrier.

- Thickness: 80~120um
- L/S, 20/20um
- With SPCC Frame and 10um Cu
• **2L MIS Package**

- Package with 2L MSAP substrate

- Package with 2L MIS substrate

### Device Information

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<tr>
<td><strong>Package Size</strong></td>
<td>12.1x13.3mm</td>
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<tr>
<td><strong>Package Thickness</strong></td>
<td>0.77mm (MSAP)</td>
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<tr>
<td></td>
<td>0.66mm (MIS)</td>
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<td><strong>Dual Die Size</strong></td>
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<td><strong>Bump#</strong></td>
<td>CuP 709 &amp; 273</td>
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<td><strong>Min. Bump Pitch</strong></td>
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<td><strong>Bump Height</strong></td>
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<td><strong>Ball count</strong></td>
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<td><strong>Ball Pitch</strong></td>
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<td><strong>Substrate layers</strong></td>
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<tr>
<td><strong>L/S</strong></td>
<td>25um/25um</td>
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### 2L MIS substrate advantage:
- Single material
- Thinner
- Low Warpage
- Achieve MSL 1
• **3L MIS Package**

✔ **Package with 4L SAP substrate**

✔ **Package with 3L MIS substrate**

<table>
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<tr>
<th>Device Information</th>
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<tbody>
<tr>
<td><strong>Package Size</strong></td>
<td>13x13mm</td>
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<tr>
<td><strong>Package Thickness</strong></td>
<td>1.0mm(SAP) 0.83mm(MIS)</td>
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<tr>
<td><strong>Die Size</strong></td>
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<td><strong>Min. Bump Pitch</strong></td>
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<td><strong>Ball Pitch</strong></td>
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<td><strong>Substrate layers</strong></td>
<td>4L(SAP) 3L(MIS)</td>
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<tr>
<td><strong>L/S</strong></td>
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**3L MIS substrate advantage:**
- Single material
- Thinner
- Low Warpage
- Achieve MSL 1
• **3D MIS Package**

✓ **3D MIS Substrate Structure**

![Diagram showing 3D MIS Substrate Structure]

✓ **3D MIS Application**

**Case 1: DC-DC Power Package**

- **Technical Features**
  - Flip chip process
  - Multiple Chips Solution
  - 3D stack Assembly Structure
  - SMT Process
  - Component Type: Resistors, Capacitors, Inductor
  - MSL 1
  - Package Qualified on 2x1.5mm

**IC+Stacked Inductor+3D MIS**
Case 2: PCM comparison with Clip Bond technology

MOSFET+IC+3D MIS

Technical Features

- DB and WB
- Multiple Chips Solution
- RDL after mold
- Superior electrical and thermal performance
- Micro PMP
- High reliability performance

Cross Section
• MIS SIP Module Package

✓ RF SIP Module

Characteristic:
• Design “Pre-plating Cu Stud” for passive components mounting area due MIS embedded trace
• Flip chip with Cu Bumping
• Coil inductance
• High reliability performance

QFN-MIS 7x6-30L

A-A

Cu Pillar Bump for Flip Chip

A-A Pre-plating Stud for SMT
• **MIS SIP Module Package**

- PMP SIP Module

**Characteristic**
- Passive Components
- Multi-chip Module
- 3D SIP
- Without Clip Bond
- Large Area Metal and Partial Finer Line/Space

**Advantages**
- Superior electrical and thermal performance
- Micro PMP
- High reliability performance
**Summary**

MIS Technology can provide

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
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<tbody>
<tr>
<td>Ultra thin package</td>
<td>X2: 0.33mm package</td>
</tr>
<tr>
<td>Multilayer package</td>
<td>2L &amp; 3L MIS package</td>
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<tr>
<td>3D MIS package</td>
<td>With 3D MIS substrate</td>
</tr>
<tr>
<td>MIS SIP module</td>
<td>IC/IDP/Passive Component/MOSFET</td>
</tr>
<tr>
<td>High reliability</td>
<td>MSL 1</td>
</tr>
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</table>
Thank You!